[GRID ARRAY PACKAGED INTEGRATED CIRCUIT]

Abstract of Disclosure

A grid array packaged integrated circuit includes a substrate and a chip with a core circuit. The chip is disposed on the substrate. The chip includes I/O devices, bonding pad arranged on the chip in a multi-tier manner surrounding the I/O devices, metal traces and vias on metal layers of the chip for electrically connecting each I/O device and each bonding pad, rings and fingers surrounding the chip on the substrate, and bonding wires for electrically connecting each bonding pad to a corresponding finger or to a corresponding ring. Bonding pads electricaly connected to different voltage levels can share the same I/O device.